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Please find below and/or attached an Office communication concerning this application or proceeding.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/774,178
Filing Date: February 06, 2004
Appellant(s): YEUNG ET AL.

Eric S. Hiponia (Reg. No. 62,002)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/08/2010 appealing from the Office action mailed 4/27/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-4, 7, 10-15, 19, 39-40.

Cancellation of claims 44 and 46-49 filed on 10/29/2010 has been entered by the examiner for purpose of simplification for appeal.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has a comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. There was a typographical error in the ground of rejection of claims 7 and 10. The corrected ground of rejection of claims 7 and 10:

Claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles as applied to claim 1 above, and further in view of U.S. Patent No. 4,811,208 of Myers et al., (hereinafter "Myers").

Claim 10 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles and Myers, as applied to claim 7 above, and further in view of U.S. Patent Application Publication No. 2002/0188884 of Jain et al (hereinafter "Jain").

Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION." Claims 44 and 46-49 has been cancelled for purpose of simplification for appeal.

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. The rejection of claims 1-4, 7, 10-11, 14-15, and 39-40 under 35 U.S.C. 112.

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

U.S. Patent Application Publication No. 2003/0115428 by Zaccarin et al.

U.S. Patent Application Publication No. 2001/0056456 by Cota-Robles

U.S. Patent No. 6,662,203 by Kling et al.

U.S. Patent No.4,811,208 by Myers et al.

U.S. Patent Application Publication No. 2002/0188884 by Jain et al.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 11-14, 19, and 39 were rejected under 35 U.S.C. § 103(a)as being unpatentable over U.S. Patent Application Publication No. 2003/0115428 of Zaccarin et al. (hereinafter "Zaccarin"), in view of U.S. Patent Application Publication No. 2001/0056456 of Cota-Robles (hereinafter "Cota-Robles").

Claims 2-4, 15, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles, and further in view of U.S. Patent No. 6,662,203 of Kling et al., (hereinafter "Kling").

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles as applied to claim 1 above, and further in view of U.S. Patent No. 4,811,208 of Myers et al., (hereinafter "Myers").

Claim 10 was also rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles and Myers, as applied to claim 7 above, and further in view of U.S. Patent Application Publication No. 2002/0188884 of Jain et al (hereinafter "Jain").

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12-13, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lacks antecedent basis:

   i. The buffer level- claim 12 & 19.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 11-14, 19, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Cota-Robles (US 2001/0056456 A1).

As per claim 1, Zaccarin teaches the invention substantially as claimed including a method, comprising:

monitoring a state of an application running in a system and a buffer associated with the multithreaded application, wherein each thread includes one or more activities to be executed by the system ([0013]; par. [0014], lines 15-23; par. [0015], lines 4-12; par. [0017]; par. [0019]; par. [0021]);

determining the buffer ([0013]; par. [0014]; par. [0015]; par. [0019]; par. [0020]); wherein at least one of the threads is associated with the application (par. [0013; par. [0014]; par. [0015]);

coordinating the dispatch of threads of the multi-threaded application (par. [0013]-par. [0016]; par. [0019]-par. [0020]; wherein variation in processor frequency/voltage change the rate at which the threads are dispatched based on buffer level or application constraint);

dynamically adjusting one or more of the frequency or voltage applied to the processor based at least in part on the availability of the buffer and the coordination of the dispatch of the threads(par. [0015]-par. [0017]); and

dynamically adjusting the buffer size based at least in part on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads (par. [0015]; par. [0017]; par. [0019]).

Zaccarin does not explicitly teach determining the availability of a processor to perform simultaneous multi-threading, coordinating the dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based at least in part on the availability of the buffer.

However, Cota- Robles teaches availability of a processor to perform simultaneous multi-threading and coordinating the dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system (abs.; par. [0022]; par. [0025]; par. [0027]).

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin and Cota-Robles because Cota-Robles teaching of SMT scheduling and coordinating the dispatching of the threads would increase system throughput and make better use of the processor.

The combined teaching does not explicitly teach the coordination of dispatching of threads of the multi-threaded application based at least in part on the availability of the buffer and determine the availability of a processor.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching that in order to dispatch the threads, one must determine first if there is any processor available for executing the threads and it is obvious according to Zaccarin teaching that changing the frequency/voltage of the processor based on the availability of the buffer is coordinating the dispatch of the threads by changing the dispatching rate based on the availability of the buffer as claimed.

As per claim 11, Zaccarin teaches said monitoring the buffer associated with the multi-threaded application includes monitoring buffer fullness levels of the buffer (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16;par. [0016], lines 10-12; par. [0018]).

As per claim 12, Zaccarin teaches said monitoring the buffer fullness levels includes, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark (par. [0015], lines 8-16; Par. [0017]; par. [0018]).

As per claim 13, Zaccarin teaches said comparing the buffer level includes determining buffer overflow and buffer underflow conditions based at least in part, on the high level mark

and the low level mark. (Par. [0015], lines 4-16; par. [0017], lines 4-15; par. [0018]-par. [0019]).

As per claim 14, it is the computer readable storage medium of the method claim 1. Therefore, it is rejected under the same rational.

As per claim 19, Zaccarin teaches monitoring the buffer associated with the multi-threaded application includes monitoring buffer fullness levels of the buffer and wherein monitoring the buffer fullness levels includes, comparing a buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark (par. [0013], lines 11-12; par. [0014], lines 10-23; par. [0015], lines 8-16; par. [0016], lines [10-12]; par. [0017]; par. [0018]).

As per claim 39, Zaccarin teaches a system, comprising:

a memory to store data and instructions (fig. 4,42; par. [0042);

a processor ; said processor operable to perform instructions (fig. 4, 56);

monitor a state of an application running in a system buffer associated with the multi-threaded application; wherein each thread includes one or more activities to be executed by the system (par. [0013]- Par. [0014]);

determining the availability of a buffer ([0013]; par. [0014]; par. [0015]; par. [0019]; par. [0020]);

coordinating the dispatch of threads of the multi-threaded application (par. [0013]-par. [0016]; par. [0019]-par. [0020]; wherein variation in processor frequency/voltage change the rate

at which the threads are dispatched based on buffer level or application constraint);

dynamically adjusting one or more of the frequency or voltage applied to the processor based at least in part on the availability of the buffer and the coordination of the dispatch of the threads(par. [0015]-par. [0017]); and

dynamically adjusting the buffer size based at least in part on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads (par. [0015]; par. [0017]; par. [0019]).

Zaccarin does not explicitly teach a processor coupled to said memory on a bus, said processor to include: a bus unit to receive a sequence of instructions from said memory; an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions, determining the availability of a processor to perform simultaneous multi-threading, coordinating the dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based at least in part on the availability of the buffer.

However, Cota- Robles teaches a bus unit to receive a sequence of instructions from said memory; an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions (fig. 1; par. [0034]), availability of a processor to perform simultaneous multi-threading and coordinating the dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system (abs.; par. [0022]; par. [0025]; par. [0027]).

It would have been obvious to one ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin and Cota-Robles because Cota-Robles teaching of SMT scheduling and coordinating the dispatching of the threads would increase system throughput and make better use of the processor.

The combined teaching does not explicitly teach the coordination of dispatching of threads of the multi-threaded application based at least in part on the availability of the buffer and determine the availability of a processor.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to conclude from the combined teaching that in order to dispatch the threads, one must determine first if there is any processor available for executing the threads and it is obvious according to Zaccarin teaching that changing the frequency/voltage of the processor based on the availability of the buffer is coordinating the dispatch of the threads by changing the dispatching rate based on the availability of the buffer as claimed.

Claims 2-4, 15, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Cota-Robles (US 2001/0056456 A1), and further in view of Kling et al. (US 6,662,203 B 1).

As per claim 2, the combined teaching of Zaccarin and Cota-Robles does not explicitly teach controlling the dispatch of the threads of the multi-threaded application in the system

includes assessing execution readiness of the one or more activities of each thread.

However, Kling teaches said controlling the dispatch of the threads of the multi-threaded application in the system includes assessing execution readiness of the one or more activities of each thread. (abs; col. 9, lines 35-67; col. 10, lines 1-9; fig. 5, 77).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Cota-Robles and kling because Kling teaching of accessing readiness of the one or more activities would improve system dispatching techniques and increase efficiency in dispatching technique of the system since one would only be dispatching ready activities only which improve the performance of the system.

As per claim 3, Kling teaches said controlling the dispatch of the threads of the multi-threaded application includes delaying a ready-to-be-dispatched activity from being dispatched (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1-15).

As per claim 4, Zaccarin teaches the first and second activities are from one or more applications (par. [0012]; par. [0021]).

The combined teaching of Zaccarin, and Cota-Robles does not explicitly teach that a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities can be dispatched together.

However, Kling teaches a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities can be dispatched together.

As per claim 15, it is the computer readable medium of the method claim 3. Therefore it is rejected under the same rational.

As per claim 40, the combined teaching of Zaccarin and Cota-Robles does not explicitly teach that said controlling the dispatch of the threads of the multi-threaded application includes delaying a ready- to-be-dispatched thread from being dispatched.

However, Kling teaches said controlling the dispatch oft of the threads of the multi-threaded application includes delaying a ready-to-be-dispatched thread from being dispatched (abs.; col. 1, lines 66- col. 2, lines 1-16; col. Col. 3, lines 58-col. 4, lines 1-24; col. 9, lines 38-col. 10, lines 1- 15; fig. 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Cota-Robles and kling since Kling teaching of delaying a ready-to-be- dispatched thread from being dispatched would improve system throughput and increase efficiency of system resource usage.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US

2003/0115428 A1), in view of Cota-Robles (US 2001/0056456 A1), as applied to claim 1 above and further in view of Myers et al. (US 4,811,208).

As per claim 7, Zaccarin teaches coordinating dispatch of the threads of the multi-threaded application is further based on the availability of the configurable hardware components (par. [0013]-par.[0020]).

The combined teaching of Zaccarin and Cota-Robles does not explicitly teach teaches the configurable hardware components including arithmetic logic unit (ALU), and registers in the system, wherein coordinating dispatch of the threads of the multi-threaded application is further based on the availability of the configurable hardware components.

However, Myers teaches the configurable hardware components including arithmetic logic unit (ALU), and registers in the system, wherein coordinating dispatch of the threads of the multi-threaded application is further based on the availability of the configurable hardware components (abs.; col. 1, lines 35-56; col. 3, lines 1-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Zaccarin, Cota-Robles and Myers because Myers teaching expand the configurable hardware in the system.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zaccarin et al. (US 2003/0115428 A1), in view of Cota-Robles (US 2001/0056456 A1) and in view of Myers et

al. (US 4,811,208) as applied to claim 7 above, and further in view of Jain et al. (US 2002/0188884 A 1).

As per claim 10, the combined teaching of Zaccarin, Cota-Robles and Myers does not explicitly teach that said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system.

However, Jain teaches said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system (par. [0040]; claim 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Zaccarin, Cota-Robles, Myers and Jain because Jain teaching of said increasing or decreasing the resources in the system includes powering on or powering off at least a portion of circuitry in the system would improve system energy consumption and increase efficiency.

(10) Response to Argument

(a) In the remarks [pg. 10-11], as per claims 1, 11-14, 19 and 39, Appellant argues that the references of Zaccarin et al. (US 2003/0115428 A1) and Cota-Robles (US 2001/0056456 A1), alone and in combinations fail to teach adjusting a buffer size. Instead, argues that Zaccarin teaches buffer levels may change but the buffer size is always fixed and cannot be changed.

(b) In the remarks [pg. 11-12], as per claims 2-4, 15 and 40 also argues that Kling fails to cure the deficiency of Zaccarin and Cota-Robles with respect to claims 1, 14 and 39 discussed above.

(c) In the remarks [pg. 12], as per claims 7, also argues that Myers fails to cure the deficiency of Zaccarin and Cota-Robles with respect to claim 1 discussed above.

(d) In the remarks [pg. 12], as per claims 10, also argues that Jain fails to cure the deficiency of Zaccarin, Cota-Robles and Myers with respect to claim 1 discussed above.

Examiner respectfully disagrees with the appellant:

In response to Appellant's argument as to pint (a) that the teaching of Zaccarin and Cota-Robles alone and in combinations fail to teach adjusting a buffer size, Appellant points in his appeal brief to specification par. [0032], as it teaches the limitation of "dynamically adjusting the buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads.". Par. [0032] of the specification points to Fig. 3A and 3B that teaches that when there is constraints on the incoming and outgoing data rates, the buffer monitoring operations maybe used to manage system resources. Par. [0032] further recites that depending on the buffer fullness levels of the buffer, the requirement for the resources in the system maybe be different by increasing or deceasing processor frequency/ voltage. Likewise, Zaccarin teaches adjusting processor clock speed (i.e. frequency) or voltage based on the monitored data buffer level which will results in adjusting data buffer level. Also, teaches that a buffer level is adjusted in accordance of application parameter (i.e. rate) and processor voltage or frequency (par. [0015]).More specifically, adjusting processor voltage or frequency will affect the application rate (par. [0014]). Par. [0032] of the appellant specification

teaches when the buffer level 310 of the buffer 305 indicates that the amount of data in the buffer is either low (below the low level mark L1) or normal (between the low level mark L1 and the high level mark H1) and the buffer level 320 of the buffer 315 indicated that the data in the buffer is high (above the high level mark H2), the requirement for resources may be reduced to reduce the second rate. For example, decreasing the frequency or the voltage applied to the processor which enables the software application to write the data in the buffer at a slower second rate to protect the buffer from a potential overflow condition. Likewise, Zaccarin teaches that depending on different buffer levels, the processor frequency is changed. For example par. [0017-0020] teaches a processor having three different frequency states that is changes based on the buffer levels (B0, B1, B2, B3). Adjusting the buffer level is a function of specific software rate, application or processor monitored and controlled and voltage/frequency changes.

In response to appellant argument that the claim limitation recites "adjusting buffer size" and that the size of the buffer in the cited art is fixed. Examiner interprets buffer size as buffer level in light of the specification and specifically in light of par. [0032] of the specification that was pointed to by the appellant in the brief, wherein states that the buffer levels are adjusted not the actual physical buffer size. Thus based on all the evidence listed above, the combined teaching of Zaccarin and Cota-Robles teaches "dynamically adjusting the buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads." as claimed.

As to point (b-d), it is clearly proven that the combined teaching of Zaccarin and Cota-Robles teaches adjusting a buffer size/level as claimed as such all dependent claims are thus considered addressed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/C. A./

Examiner, Art Unit 2195

Conferees:

/Emerson C Puente/

Supervisory Patent Examiner, Art Unit 2196

/Lewis A. Bullock, Jr./

Supervisory Patent Examiner, Art Unit 2193